WHAT IS CLAIMED IS:

1. A double data rate memory controller, comprising:

a plurality of data and strobe pads;

means for receiving data and strobe signals via said pads at 1x double data rate memory speed; and

means for receiving data and strobe signals via said pads at Mx double data rate memory speed ($M \geq 2$).

2. The double data rate memory controller of claim 1, further comprising:

means for reading a data width from each of a number of memory devices coupled to said memory controller; and

means for associating ones of said strobe pads with ones of said data pads when communicating with said memory devices, in one or more of a plurality of data/strobe ratios supported by the memory controller, and in data/strobe ratio(s) determined by said data width(s) read from said number of memory devices.

3. The double data rate memory controller of claim 1, further comprising:

means for writing data and generating strobes via said pads at 1x double data rate memory speed; and

means for writing data and generating strobes via said pads at Mx double data rate memory speed.

4. The double data rate memory controller of claim 3, further comprising:

means for reading a data width from each of a number of memory devices coupled to said memory controller; and

means for associating ones of said strobe pads with ones of said data pads when communicating with said memory devices, in one or more of a plurality of data/strobe ratios supported by the memory controller, and in data/strobe ratio(s) determined by said data width(s) read from said number of memory devices.

5. A memory controller, comprising:

a plurality of data pads and strobe pads, wherein data is read and written at each of said data pads in sync with a strobe that is received at or generated by a corresponding one of said strobe pads;

for each data pad, receiver circuitry comprising P storage elements, wherein i) in a first mode, data bits stored by the P storage elements are multiplexed to generate a single data stream, and ii) in a second mode, data bits stored in the P storage elements are multiplexed to generate at least two data streams; and

for each strobe pad, receiver circuitry comprising a counter to count received strobe edges; wherein particular counts of strobe edges received at a particular strobe pad cause data to be received by particular ones of the P storage elements associated with data pads corresponding to the particular strobe pad.

6. The memory controller of claim 5, wherein each of said storage elements is a latch.

7. The memory controller of claim 5, wherein each of said storage elements is a flip-flop.

8. The memory controller of claim 5, wherein each of said counters is a rollover counter which produces said count as a P bit, one-high count.

9. The memory controller of claim 5, wherein P=4.

10. The memory controller of claim 5, wherein the at least two data streams consist of even and odd data streams.

11. The memory controller of claim 5, further comprising:

a clock generation circuit to generate strobes at said strobe

pads at a 1x rate when the memory controller is configured in said first mode, or at an Mx rate when the memory controller is configured in said second mode;

for each data pad, driver circuitry to alternately couple ones of a corresponding subset of N data propagation circuits to the data pad, thereby driving a merged data stream to the data pad; and

circuitry to, i) in said first mode, provide like data input streams to each of the N data propagation circuits associated with a given data pad, and ii) in said second mode, provide different data input streams to each of the N data propagation circuits associated with a given data pad.

12. The memory controller of claim 11, wherein for each data pad, said driver circuitry comprises N sequentially clocked flip-flops which respectively receive and output data from the N data propagation circuits.

13. The memory controller of claim 11, wherein for each data pad, said driver circuitry comprises a multiplexer which receives and sequentially outputs data from the N data propagation circuits.

14. The memory controller of claim 11, wherein for each data pad, said driver circuitry comprises N tri-statable paths which respectively receive and sequentially output data from the N data propagation circuits.

15. The memory controller of claim 5, further comprising a memory to store indications of data/strobe ratios that are required to access memory devices that are coupled to said data and strobe pads of the memory controller; wherein, for a data transmission initiated with a particular one of the memory devices, a number of said data pads is dynamically associated with a number of said strobe pads, in

response to a corresponding indication of a data/strobe ratio stored in the memory.

16. A computer system, comprising:

a CPU;

a memory controller coupled to said CPU; and

a number of memory devices coupled to said memory controller;

wherein said memory controller comprises:

a plurality of data pads and strobe pads coupled to said memory devices, wherein data is read and written at each of said data pads in sync with a strobe that is received at or generated by a corresponding one of said strobe pads;

for each data pad, receiver circuitry comprising P storage elements, wherein i) in a first mode, data bits stored by the P storage elements are multiplexed to generate a single data stream, and ii) in a second mode, data bits stored in the P storage elements are multiplexed to generate at least two data streams; and

for each strobe pad, receiver circuitry comprising a counter to count received strobe edges; wherein particular counts of strobe edges received at a particular strobe pad cause data to be received by particular ones of the P storage elements associated with data pads corresponding to the particular strobe pad.

17. The computer system of claim 16, wherein each of said counters is a rollover counter which produces said count as a P bit, one-high count.

18. The computer system of claim 16, further comprising:

a clock generation circuit to generate strobes at said strobe pads at a 1x rate when the memory controller is configured in said first mode, or at an Mx rate when the memory controller is configured in said second mode;

for each data pad, driver circuitry to alternately couple ones of a corresponding subset of N data propagation circuits to the data pad, thereby driving a merged data stream to the data pad; and

circuitry to, i) in said first mode, provide like data input streams to each of the N data propagation circuits associated with a given data pad, and ii) in said second mode, provide different data input streams to each of the N data propagation circuits associated with a given data pad.

19. The computer system of claim 16, further comprising a memory to store indications of data/strobe ratios that are required to access memory devices that are coupled to said data and strobe pads of the memory controller; wherein, for a data transmission initiated with a particular one of the memory devices, a number of said data pads is dynamically associated with a number of said strobe pads, in response to a corresponding indication of a data/strobe ratio stored in the memory.